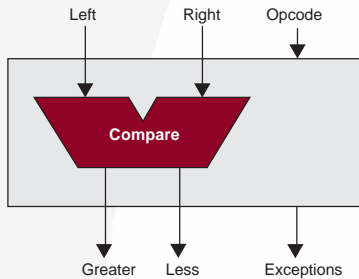


Floating Point compare unit



Features

- IEEE Single Precision Floating Point Compare
- IEEE-like Single Precision Floating Point Compare (Denormals treated as Zeros)
- Fully Combinational Design

Description

The Floating Point Compare Unit supports two operations:

- IEEE-Compliant Floating Point Compare
- Non-IEEE-Compliant Floating Point Compare

The IEEE compliant Compare operation follows the IEEE 754 Standard for Floating Point Arithmetic for Single Precision (32-bit) arithmetic.

The non-IEEE compliant operation follows the IEEE 754 Standard for Floating Point Arithmetic for Single Precision (32-bit) arithmetic with the exception that Denormals are treated as like-signed Zeros. An additional exception flag is provided to signal when a Denormal input is flushed to Zero.

Compare results are encoded on two outputs: Greater, and Less. When both are active, the Unordered case is signaled. When neither is active, the Equal case is signaled.

The Floating Point Compare Unit is a fully combinational unit. The design is coded in a pipelined fashion, and pipeline registers may be easily added.

The approximate gate count and latency for the Floating Point Compare unit is 500 gates and 1.0 ns for a typical 0.18 micron Standard Cell technology.

Applications

- Microcontrollers
- Microprocessors



Silicon Logic Engineering

Phone: (715) 830-1200 • Fax: (715) 830-1887
Email: sales@siliconlogic.com