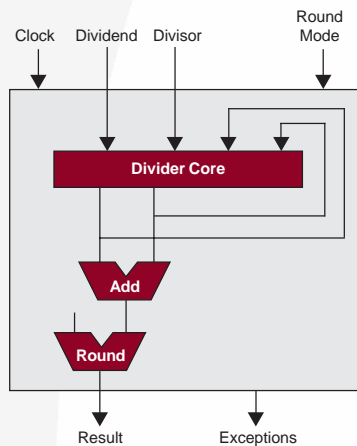


Floating Point divide unit



Features

- IEEE-like Arithmetic (Denormals treated as Zeros)
- IEEE Single Precision Format
- Fully Synchronous Design
- All outputs registered
- Minimal combinational logic on inputs
- 15-clock pipeline rate
- 17-clock latency

Description

The Floating Point Divide Unit is optimized to exclusively support the divide operation.

The operation of this unit follows the IEEE 754 Standard for Floating Point Arithmetic for Single Precision (32-bit) arithmetic with the exception that Denormals are treated as like-signed Zeros. An additional exception flag is provided to signal when a Denormal input or what would have been a Denormal output is flushed to Zero. Results for exceptions are the IEEE Standard default results as defined for the case when no trap occurs.

The Floating Point Divide Unit divider core uses an SRT algorithm to provide two quotient bits per clock cycle. A go signal causes the unit to reset, capture the input operands, and to begin the division process. A done signal is provided to signal that the result is ready. The done signal can be configured to appear immediately when a Zero, QNaN, or Infinity result can be determined directly from the input operands.

The signaling of Underflow is configurable for the detection of tininess either before or after rounding.

This block is optimized to provide two quotient bits per clock, and is partially pipelined to maximize throughput. All inputs and outputs of this block are registered, except that the input registers have holding multiplexers in front of them; there is no logic after the output registers.

The latency of this unit is 17 clocks, and the pipeline rate is 15 clocks, with an early termination option. The approximate gate count and peak clock frequency for the Floating Point Divide Unit is 5,300 gates and 333 MHz for a typical 0.18 micron Standard Cell technology. This gate count includes 279 flip-flops.

Applications

- Microcontrollers
- Microprocessors



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