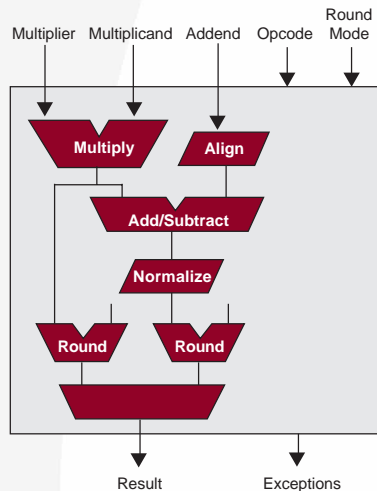


# Floating Point multiply accumulate unit

## Description

The Floating Point Multiply Accumulate Unit supports three operations:

- Floating Point Multiply Add
- Floating Point Multiply Subtract
- Floating Point Multiply



The Floating Point Multiply Accumulate Unit is optimized to support multiply-accumulate operation, with a bypass for the standard Multiply operation to provide a potentially lower latency.

The operation of this unit follows the IEEE 754 Standard for Floating Point Arithmetic for Single Precision (32-bit) arithmetic with the exception that Denormals are treated as like-signed Zeros. An additional exception flag is provided to signal when a Denormal input or what would have been a Denormal output is flushed to Zero. Results for exceptions are the IEEE Standard default results as defined for the case when no trap occurs.

The Floating Point Multiply Unit is a fully combinational unit. The design is coded in a pipelined fashion, and pipeline registers may be easily added to support higher clock frequencies.

A bypass path is provided to speed up Floating Point Multiply. This is especially valuable if pipeline registers are added.

The Multiply Add and Multiply Subtract operations are fused operations which have only one rounding error. There are two configurable modes for signaling Invalid for these operations. In one mode, a QNaN addend will block an Invalid due to a multiplication of Zero by Infinity. In the other mode, exceptions are computed as if the multiplication and addition were separate operations.

NaN formats may be specified with a configurable QNaN bit value and bit position, and a default QNaN may be specified for Invalid results.

The signaling of Underflow is configurable for the detection of tininess either before or after rounding.

The approximate gate count and latency for the Floating Point Multiply Accumulate unit is 12,800 gates and 12.5 ns for a typical 0.18 micron Standard Cell technology.

## Features

- IEEE-like Arithmetic (Denormals treated as Zeros)
- IEEE Single Precision Format
- Fully Combinational Design

## Applications

- Microcontrollers
- Microprocessors



**Silicon Logic Engineering**

Phone: (715) 830-1200 • Fax: (715) 830-1887  
Email: sales@siliconlogic.com