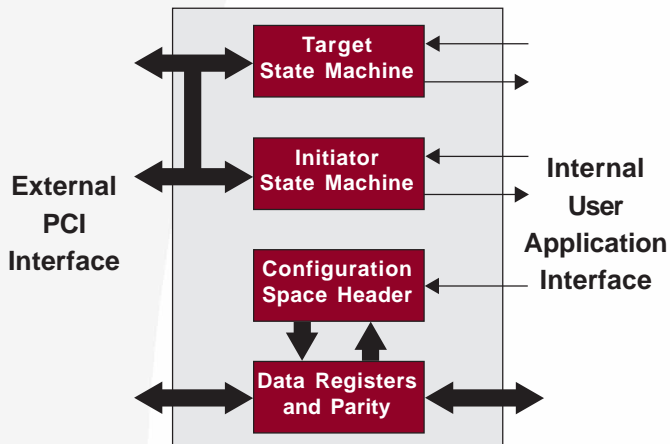


# PCI Core interface block



## Description

The PCI Core is a highly configurable interface block to allow efficient communication between a PCI 2.2 Local Bus and User Application logic. Both 64-bit and 32-bit implementation options are supported.

## Features

- Fully compliant with the PCI Local Bus Specification, Revision 2.2
- Technology-independent core bundled with a separate wrapper for technology-specific I/O buffers
- Target-Only or Initiator-Target options
- 32-bit or 64/32-bit options
- 0-66 MHz operating frequency depending on implementation technology
- Flexible user interface that can be configured for many applications
- Medium Speed DEVSEL Decode
- Type 0 Configuration Space Header
- Up to three 32-bit Base Address Registers
- Supports User Configuration Space
- Self Configuration Read and Write commands supported



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