

The logo for ASICBlaster™ toolsuite. 'ASICBlaster™' is in a white, bold, sans-serif font. 'toolsuite' is in a smaller, grey, lowercase, sans-serif font. The background is a dark blue gradient with a faint white circuit board pattern.

ASICBlaster™ toolsuite

ASICBlaster toolsuite is a suite of point tools developed in house to bridge gaps and increase productivity, enabling SLE to be more efficient and to achieve better results on leading-edge designs. Each tool addresses a specific problem within the ASIC design process. The tools are optimized to work on large, high-speed ASIC designs.

They are designed to work with, not compete against, existing industry-standard ECAD tools.

Featuring ScanBlaster™

ScanBlaster is a scan insertion utility that gives users the features needed to enable scan insertion on large, complex designs without compromising performance. ScanBlaster is uniquely positioned to be able to account for physical effects early, and to be compatible with many of the standard test insertion methodologies in use. It is especially well suited to handling large, high-speed designs with unique testability requirements.

ScanBlaster relies on other industry standard test insertion tools for the basic functions they provide, and supplements their functionality. It adds benefits that currently are not available in these tools; it is not designed as a replacement for these tools.

Benefits

- Tcl interface for several industry-standard tools
- Design partitioning into 'chipllets' (small physically local regions) to give better performance, less congestion, and better timing
- SCAN_IN and SCAN_OUT pins are used as anchors to help determine ordering of scan chains to avoid unnecessarily long scan routes
- Register placement information can be used to control scan insertion down to the register level if desired
- On-chip memory structures are dealt with separately to allow user to control how their scan chains are connected with other scan elements
- Registers within different clock domains can be easily isolated to minimize the number of resynchronization flops required
- Test logic and functional logic can be isolated (e.g., boundary scan or BIST logic)
- Scan tracing function is useful for planning scan architecture.
- Scan connections to pre-wired chains or to custom cores and blackboxes supported via attributes on the designs
- Muxed-scan flip-flop and LSSD design styles supported
- Scan chain order within full or partial chains can be preserved



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